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## (54) Printed circuit board

(57) A printed circuit board (10) has a first image (11). In the first image (11) there is a first ball grid array pattern (61) for attaching a first input/output ball grid array package. The first ball grid array pattern (61) includes a de-populated center area. A first surface insulation resistance pattern (62) is laid out within the de-populated center area of the first ball grid array pattern (61). A second ball grid array pattern (24) also may be contained within the first image (11). The second ball grid array pattern (24) is for attaching a second input/output ball grid array package. The second ball grid array pattern (24) has rows of interconnect pads (81). A second surface insulation resistance pattern (82) is laid out between the rows of interconnect pads (81).

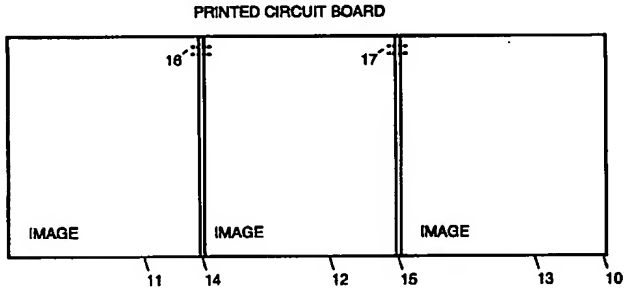


FIGURE 1

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## Description

[0001] The present invention concerns a printed circuit board for use, for example, for testing the reliability of processes performed in its construction.

[0002] Printed circuit boards are often processed using automated processing equipment. When setting up such automated processing equipment it is generally necessary to test the automated processes before using the equipment to produce printed circuit boards to be distributed commercially.

[0003] The testing generally includes checking the integrity of the soldering process. This includes assuring that when soldering parts to the printed circuit board connections are strong and reliable and that parts are not damaged during the soldering processing. Additionally, it is necessary to verify that, after cleaning is completed, the soldering joints are clean and there is no remaining contaminants which can cause shorts. Also there is a need to test the reliability of the solder joints under environmental stress conditions. If the automated test equipment is to be used with printed circuit boards of different sizes and shapes, it is necessary to perform testing on printed circuit boards which are of similar size and shape as production printed circuit boards.

[0004] In order to test automated processing equipment, test cards are often used. Existing test cards are typically fabricated with hot air solder leveling. These test cards include daisy-chain patterns. The daisy chain patterns allow for continuity testing of soldered packages. In order to perform such testing, integrated circuit packages, which are specially designed for testing automated processing equipment, are soldered to the test cards. After the assembly process is finished, an ohmeter is used to determine whether die electrical connections are complete.

[0005] While existing test cards are useful in testing automated processing equipment, the currently available cards are limited in the avaiable size of cards, are limited in package selection and are limited in the types and versatility of testing that may be performed.

[0006] According to an aspect of the present invention there is provided a printed circuit board as specified in claim 1.

[0007] According to another aspect of the present invention there is provided a printed circuit board as specified in claim 9.

[0008] In accordance with the preferred embodiment of the present invention, a printed circuit board has a first image. In the first image there is a first ball grid array pattern for attaching a first input/output ball grid array package. The first ball grid array pattern includes a de-populated center area. A first surface insulation resistance pattern is laid out within the de-populated center area of the first ball grid array pattern.

[0009] As part of the same embodiment of the present invention, or as part of an alternative embodiment, a second ball grid array pattern is within the first image. The second ball grid array pattern is for attaching a second input/output ball grid array package. The second ball grid array pattern has rows of interconnect pads. A second surface insulation resistance pattern is laid out between the rows of interconnect pads. For example, the second surface insulation resistance pattern is laid out at a 45 degree angle with respect to the rows of interconnect pads

[0010] Also in the preferred embodiment, the first image includes a third ball grid array pattern for attaching a third input/output ball grid array package, and includes a fourth ball grid array pattern for attaching a fourth input/output ball grid array package. The first image also includes a through hole connector area for receiving leads of a through hole connector, and a plurality of wagon wheel face plate connectors. This allows for a variety of types of testing using the same printed circuit board.

[0011] Within the first image, a plurality of pairs of surface mount pads are for mounting LEDs. Also, a plurality of interconnect vias are for connecting terminals of a tester during environmental testing.

[0012] The printed circuit board can include additional images. For example, the printed circuit board includes a second image which is substantially identical to the first image, and includes a third image which substantially identical to the first image and the second image.

[0013] The preferred board has significant advantages over prior art test boards. For example, the surface insulation resistance (SIR) patterns allow testing the cleanliness of the boards. The mounting of LEDs allows for visual testing without the use of an ohmmeter. The interconnect vias facilitate easy connection for environmental testing. The use of three images, which can be separated, allows the testing of test cards of different sizes. Fabricating the printed circuit using Organic Coat Copper (OCC) allows for testing of boards made with this technology. Fabricating the printed circuit using Hot Air Solder Leveling (HASL) allows for testing of boards made with this technology. Additionally, the use of multiple layers better simulates a product. The use of through hole connectors and face plate connectors which use different assembly processes also allows the tests cards to better simulate a real product.

[0014] An embodiment of die present invention is described below, by way of example only, with reference to the accompanying drawings, in which:

Figure 1 is simplified block diagram showing layout of a preferred embodiment of printed circuit board used for testing;

Figure 2 is a simplified diagram which shows connections for an image of the printed circuit board shown in Figure 1;

Figure 3 is a simplified diagram which shows a 256 input/output ball grid array pattern and a surface

insulation resistance pattern placed on the printed circuit board shown in Figure 1;

Figure 4 is a simplified diagram which shows a 324 input/output ball grid array pattern placed on the printed circuit board shown in Figure 1;

Figure 5 is a simplified diagram which shows a 313 input/output ball grid array pattern and a surface insulation resistance pattern placed on the printed circuit board shown in Figure 1;

Figure 6 is a simplified diagram which shows a 388 input/output ball grid array pattern placed on the printed circuit board shown in Figure 1; and

Figure 7 is a simplified cross section of the printed circuit board shown in Figure 1.

**[0015]** Figure 1 is a simplified diagram showing layout of a ball grid array (BGA) test board 10. BGA test board 10 is a six-layer FR-4 glass epoxy printed circuit board. BGA test board 10 is fabricated using organic coat copper (OCC). There are three sections, or images, on test board 10. Shown in Figure 1 is an image 11, an image 12 and an image 13. Each image is a duplicate of the others, except for numbering which appears on the board. In the preferred embodiment, all packages on image 11 are numbered in the tens. All packages on image 12 are numbered in the twenties. All packages on image 13 are numbered in the thirties.

**[0016]** A routing area 14 separates image 11 from image 12. Routing area 14 allows image 11 and image 12 to be separated into separate boards for individual testing. When image 11 is separated from image 12, the separation occurs at routing area 14.

**[0017]** Routing area 14 electrically isolates the VCC plane for image 11 from the VCC plane for image 12. Routing area 14 isolates the ground plane for image 11 from the ground plane for image 12 except for a single trace 16. The single trace 16 allows testing using a common ground when image 11 and image 12 remain attached.

**[0018]** Likewise, routing area 15 separates image 12 from image 13. Routing area 15 allows image 12 and image 13 to be separated into separate boards for individual testing. When image 12 is separated from image 13, the separation occurs at routing area 15.

**[0019]** Routing area 15 electrically isolates the VCC plane for image 12 from the VCC plane for image 13. Routing area 15 isolates the ground plane for image 12 from the ground plane for image 13 except for a single trace 17. The single trace 17 allows testing using a common ground when image 12 and image 13 remain attached.

**[0020]** Figure 2 shows additional detail of image 11. Image 12 and image 13 have identical layouts. As illustrated by Figure 2, four different packages can be attached to image 11. A 256 BGA input/output package can be attached to image 11 at a "256" BGA pattern 22. A 324 BGA input/output package can be attached to image 11 at a "324" BGA pattern 23. A 313 BGA input/output package can be attached to image 11 at a "313" BGA pattern 24. A 388 BGA input/output package can be attached to image 11 at a "388" BGA pattern 25.

**[0021]** A through hole connector area 21 is ready for attachment of a through hole connector. Eighty interconnect vias within a sub-area 26 are ready to receive the pins of a connector. A mounting hole 27 and a mounting hole 28 are available to secure the connector to BGA test board 10.

**[0022]** An interconnect via 41, an interconnect via 42, an interconnect via 43, an interconnect via 44, an interconnect via 47, an interconnect via 48, an interconnect via 49, an interconnect via 53 and an interconnect via 50 are each 0.050 inches in diameter and are suitable for soldering on test posts for ease of connection of test equipment.

**[0023]** Interconnect via 43 is an environmental test point for performing environmental checking the 256 BGA input/output package attached to image 11. Interconnect via 44 is an environmental test point for performing environmental checking the 324 BGA input/output package attached to image 11. Interconnect via 49 is an environmental test point for performing environmental checking the 313 BGA input/output package attached to image 11. Interconnect via 53 is an environmental test point for performing environmental checking the 388 BGA input/output package attached to image 11. Interconnect via 50 is a common environmental test point for performing environmental checking. The use of interconnect vias rather than surface pads allows for more permanent connection of probes for environmental testing.

**[0024]** Interconnect via 41 and interconnect via 42 are for checking the integrity of a surface insulation resistance (SIR) pattern (shown in Figure 3) which is placed in the de-populated center area of "256" BGA pattern 22. Interconnect via 47 and interconnect via 48 are for checking the integrity of a surface insulation resistance (SIR) pattern (shown in Figure 5), which is laid out at a 45 degree angle between the rows of interconnect pads within the area of "313" BGA pattern 24.

**[0025]** Each concentric row (or ring) of pads for a BGA input/output package, or pairs of concentric rows (rings) in the case of "313" BGA pattern 24, lead out to an LED and test pad for testing that ring independently of the other rings. Additionally, the whole set of pads is connected such that the whole package can be tested with the LED or an ohmmeter with one measurement.

**[0026]** Surface mount pads 29, surface mount pads 30, surface mount pads 31 and surface mount pads 32, are for mounting LED lights used in testing. Surface mount pads 33, surface mount pads 34, surface mount pads 35 and surface mount pads 36 are for mounting current limiting resistors.

[0027] Test pads 37 are for testing individual concentric rows of "256" BGA pattern 22. The test pad for the outer most concentric row is on the left and the test pad for the inner most concentric row is on the right. Common test pad 45 is used in conjunction with tests pads 37 to test the concentric rows of "256" BGA pattern 22. Test pads 39 are for testing individual concentric rows of "324" BGA pattern 23. The test pad for the outer most concentric row is on the left and the test pad for the inner most concentric row is on the right. Common test pad 46 is used in conjunction with test pads 39 to test the concentric rows of "324" BGA pattern 23.

[0028] Test pads 38 are for testing pairs of concentric rows of "313" BGA pattern 24. The test pad for the outer most pair of concentric rows is on the left and the test pad for the inner most pair of concentric rows is on the right. Common test pad 51 is used in conjunction with test pads 38 to test the concentric rows of "313" BGA pattern 24. Test pads 32 are for testing individual concentric rows of "388" BGA pattern 25. The test pad for the outer most concentric row is on the left and the test pad for the inner most concentric row is on the right. Common test pad 52 is used in conjunction with test pads 40 to test the concentric rows of "388" BGA pattern 25.

[0029] A wagon wheel 54, a wagon wheel 55, a wagon wheel 56 and a wagon wheel 57 are used for face plate connections.

[0030] As discussed above, there is a common ground running throughout BGA test board 10. The common ground is connected such that if the three images of BGA test board 10 are split apart, the common ground is still functional among the four packages mounted on each separate image. The common ground is electrically connected to common test pad 45, common test pad 46, common test pad 51 and common test pad 52.

[0031] Each image also has its own set of tooling holes and fiducial marks, so each individual image can be processed by itself. For example, Figure 2 shows a fiducial mark 58, a fiducial mark 59, a tooling hole 64, a tooling hole 65 and a tooling hole 66. There are also vernier alignment marks in the x-axis in the lower left and upper right corners, used for checking alignment of the paste stencil.

[0032] After the four packages, resistors and LEDs are placed, reflowed, solder waved, and washed, a visual test of the board can be done using the LEDs. The inclusion of LEDs allows for testing with a test battery rather than using an ohmmeter. To test individual concentric rows of interconnections, one lead of a three volt DC battery is attached to the common test pad for the BGA input/output package to be tested. The other lead of the battery is connected to the test point for the concentric row to be tested. If there is continuity amongst all the interconnects for that row, the LED for the concentric row will light up, showing a "good" condition.

[0033] In order to run environmental tests, one lead of an ohmmeter or other continuity measuring device is attached to a common environmental test point such as via 50. The other lead of the ohmmeter is connected to an environmental test point for the BGA input/output package to be tested. For the 256 BGA input/output (I/O) package the environmental test point is interconnect via 43. For the 324 BGA input/output package the environmental test point is interconnect via 44. For the 313 BGA input/output package the environmental test point is interconnect via 49. For the 388 BGA input/output package the environmental test point is interconnect via 53. The reading on the ohmmeter should be in the range of a fraction of an ohm if the interconnections are all good. BGA test board 10 is then exposed to environmental test conditions.

[0034] In order to run the surface insulation resistance (SIR) test, the test equipment is connected to the two SIR test points for the test. To test the SIR comb pattern placed in the de-populated center area of "256" BGA pattern 22, interconnect via 41 and interconnect via 42 are used. To test the SIR comb pattern laid out at a 45 degree angle between the rows of interconnect pads within the area of "313" BGA pattern 24, interconnect via 47 and interconnect via 48 are used. BGA test board 10 is then exposed to the environmental conditions and the SIR test can be run as per industry standard procedures.

[0035] Figure 3 shows interconnect pads 61 for "256" BGA pattern 22. Within the de-populated center area of interconnect pads 61 is a surface insulation resistance (SIR) pattern 62. SIR comb pattern 62 is used to test for cleanliness under the 256 BGA input/output (I/O) package.

[0036] Figure 4 shows interconnect pads 71 for "324" BGA pattern 23.

[0037] Figure 5 shows interconnect pads 81 for "313" BGA pattern 24. A surface insulation resistance (SIR) pattern 82 is laid out at a 45 degree angle between the rows of interconnect pads 81 within the area of "313" BGA pattern 24. SIR comb pattern 82 is used to test for cleanliness under the 313 BGA input/output (I/O) package. The unique design of SIR comb pattern 82 precludes the need to remove some of the solder balls from the middle of the 313 BGA input/output package. Removal of some of the solder balls from the middle of a BGA input/output package alters the conditions of the test from conditions which would actually occur under manufacturing and use conditions.

[0038] Figure 6 shows interconnect pads 91 for "388" BGA pattern 25.

[0039] Figure 7 illustrates the six layers of BGA test board 10. A top layer 101 is laid out as shown in Figures 1 through 6. On a layer 102 is placed solid copper which is used to simulate a ground plane. Traces are placed on a layer 103 and a layer 104 to simulate signal transmission layers. Also in layer 104, identifying marks are etched in a particular pattern, so that each of the images can be distinguished under X-ray. On a layer 105 is placed solid copper which is used to simulate a

VCC plane. Traces are placed on a layer 106. The traces are used as "stitching" which connects adjacent connectors of each BGA input/output package.

**[0040]** As will be understood by those familiar with the art, the preferred embodiment may be embodied in other specific forms.

**[0041]** The disclosures in United States patent application no. 08/986,078, from which this application claims priority, and in the abstract accompanying this application are incorporated herein by reference.

## Claims

1. A printed circuit board (10) comprising:

   a first image (11), the first image (11) comprising:

   a first array pattern (22-25) for attaching a package,
   a first power plane (105), and
   a first ground plane (102);

   a second image (12), the second image (12) comprising:

   a second array pattern (22-25) for attaching a package,
   a second power plane (105), and
   a second ground plane (102);

   a first routing area (14) between the first image (11) and the second image (12), the first routing area (14) electrically and physically isolating the first power plane (105) from the second power plane (105), the first routing area (14) also physically isolating the first ground plane (102) from the second ground plane (102); and,
   a first single trace (16) extending through the first routing area (14), the first single trace (16) electrically connecting the first ground plane (102) to the second ground plane (102).

2. A printed circuit board (10) as in claim 1 additionally comprising:

   a third image (13), the third image (13) comprising:

   a third array pattern (22-25) for attaching a package,
   a third power plane (105), and
   a third ground plane (102);

   a second routing area (15) between the second image (12) and the third image (13), the second routing area (15) electrically and physically isolating the second power plane (105) from the third power plane (105), the second routing area (15) also physically isolating the second ground plane (102) from the third ground plane (102); and,
   a second single trace (17) extending through the second routing area (15), the second single trace (17) electrically connecting the second ground plane (102) to the third ground plane (102).

3. A printed circuit board (10) as in any previous claim: wherein the first array pattern (22-25) is a first ball grid array pattern (61) for attaching a first input/output ball grid array package, the first ball grid array pattern (61) including a de-populated center area; and,
   wherein a first surface insulation resistance pattern (62) is laid out within the de-populated center area of the first ball grid array pattern (61).

4. A printed circuit board (10) as in any previous claim wherein the first image (11) additionally comprises:

   a second ball grid array pattern (24) for attaching a second input/output ball grid array package, the second ball grid array pattern (24) having rows of interconnect pads (81); and,
   a second surface insulation resistance pattern (82) laid out between the rows of interconnect pads (81).

5. A printed circuit board (10) as in claim 1, 2 or 4: wherein the first array pattern (22-25) is a first ball grid array pattern (81) for attaching a first input/output ball grid array package, the first ball grid array pattern (81) having rows of interconnect pads; and, wherein a first surface insulation resistance pattern (82) is laid out between the rows of interconnect pads.

6. A printed circuit board (10) as in any previous claim wherein the first image (11) additionally comprises:

   a plurality of pairs of surface mount pads (29-32), the plurality of pairs of surface mount-pads (29-32) being for mounting LEDs.

7. A printed circuit board (10) as in any previous claim wherein the first image (11) additionally comprises:

   a plurality of interconnect vias (37-39) for connecting terminals of a tester during environmental testing.

8. A printed circuit board (10) as in any previous claim: wherein the first image (11) includes first fiducial marks (58,59) and first tooling holes (64-66); and, wherein the second image (12) includes second

fiducial marks (58,59) and second tooling holes (64-66).

9. A printed circuit board (10) comprising:

a first image (11), the first image (11) comprising:

a first ball grid array pattern (81) for attaching a first input/output ball grid array package, the first ball grid array pattern (81) having rows of interconnect pads, and
a first surface insulation resistance pattern (82) laid out between the rows of interconnect pads.

10. A printed circuit board (10) as in claim 9 wherein the first image (11) additionally comprises:

additional ball grid array patterns (22-24) for attaching additional input/output ball grid array package.

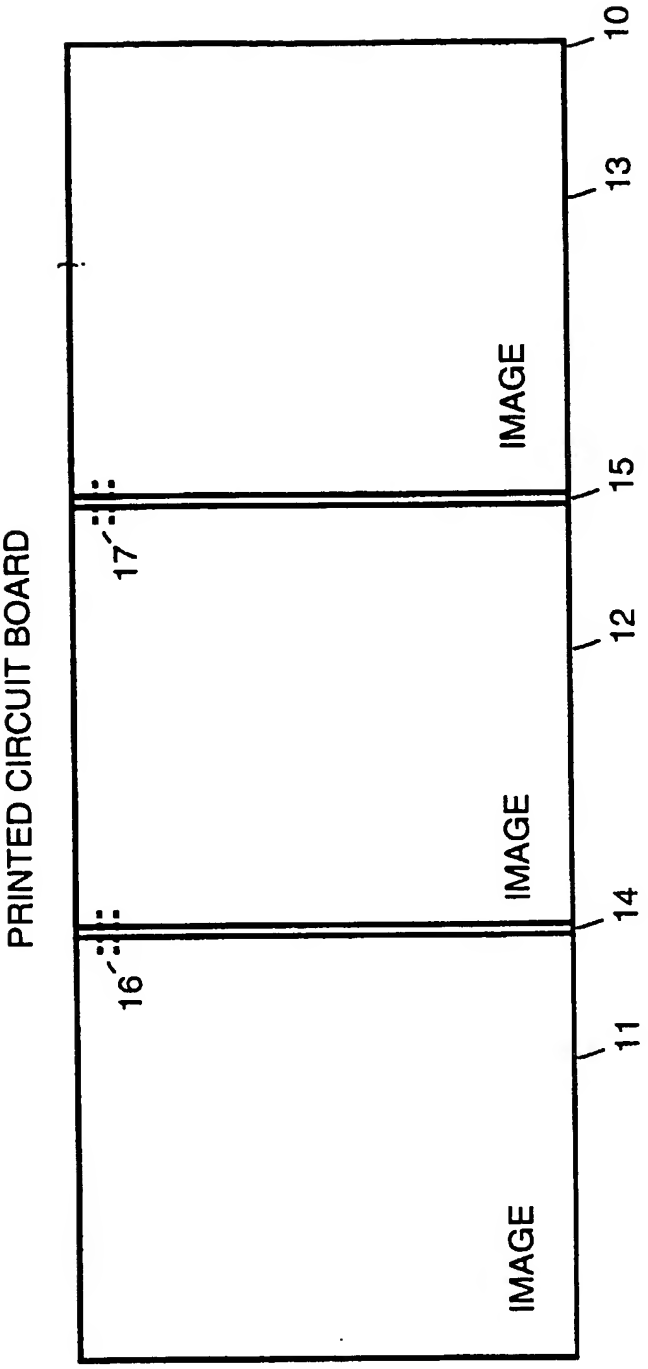
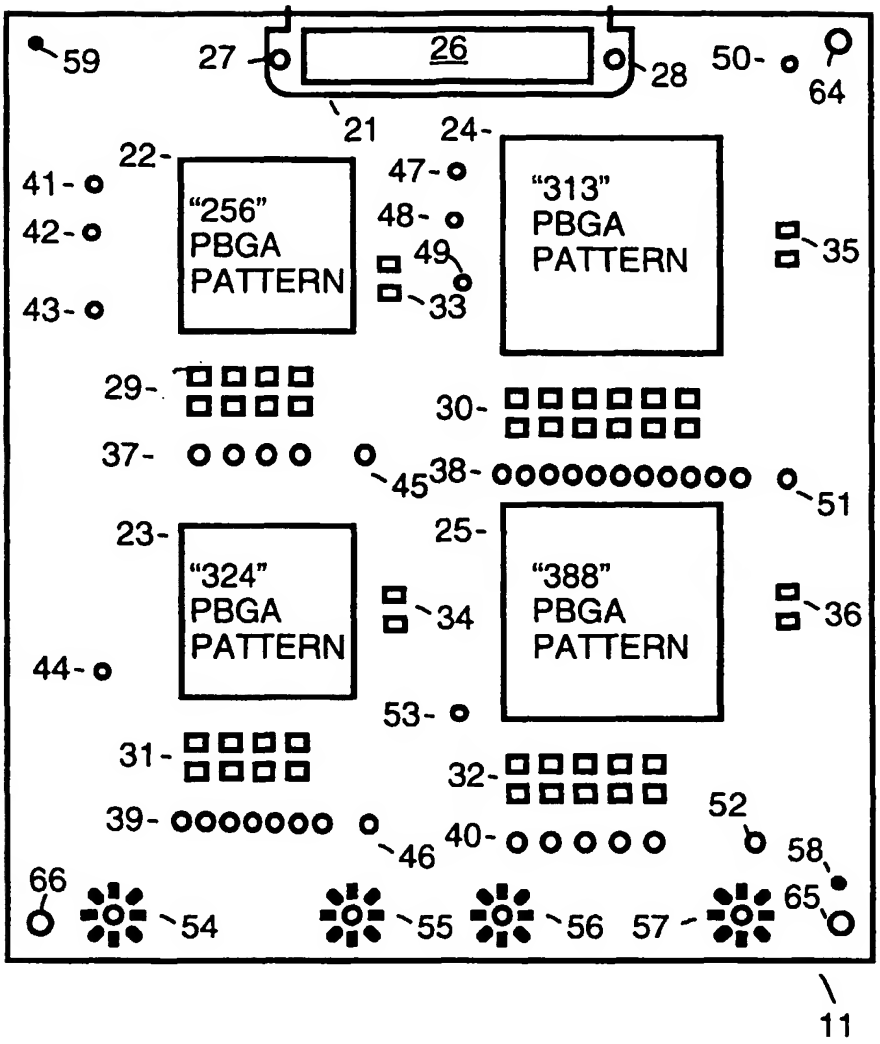

PRINTED CIRCUIT BOARD
IMAGE
IMAGE
IMAGE
10
11
12
13
14
15
16
17

FIGURE 1


59
27
26
28
50
64
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24
22
41
47
"313"
PBGA
PATTERN
"256"
PBGA
PATTERN
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48
49
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43
33
29
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45
38
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23
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"324"
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34
"388"
PBGA
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58
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65
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56
57
11

FIGURE 2

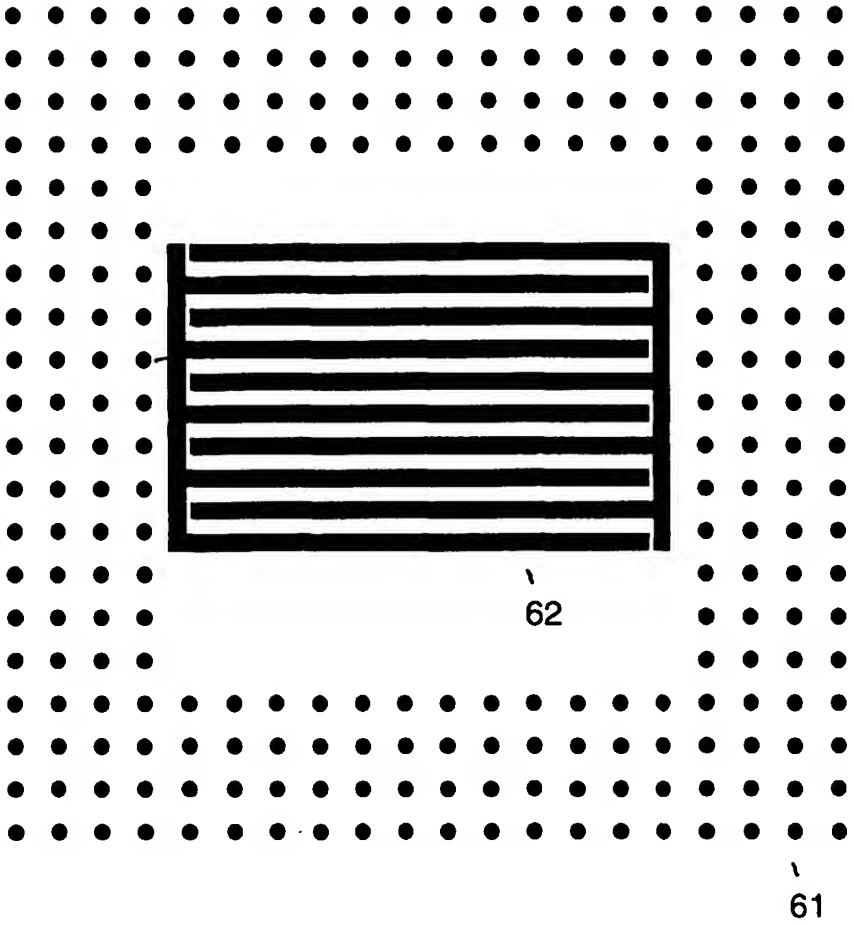


FIGURE 3

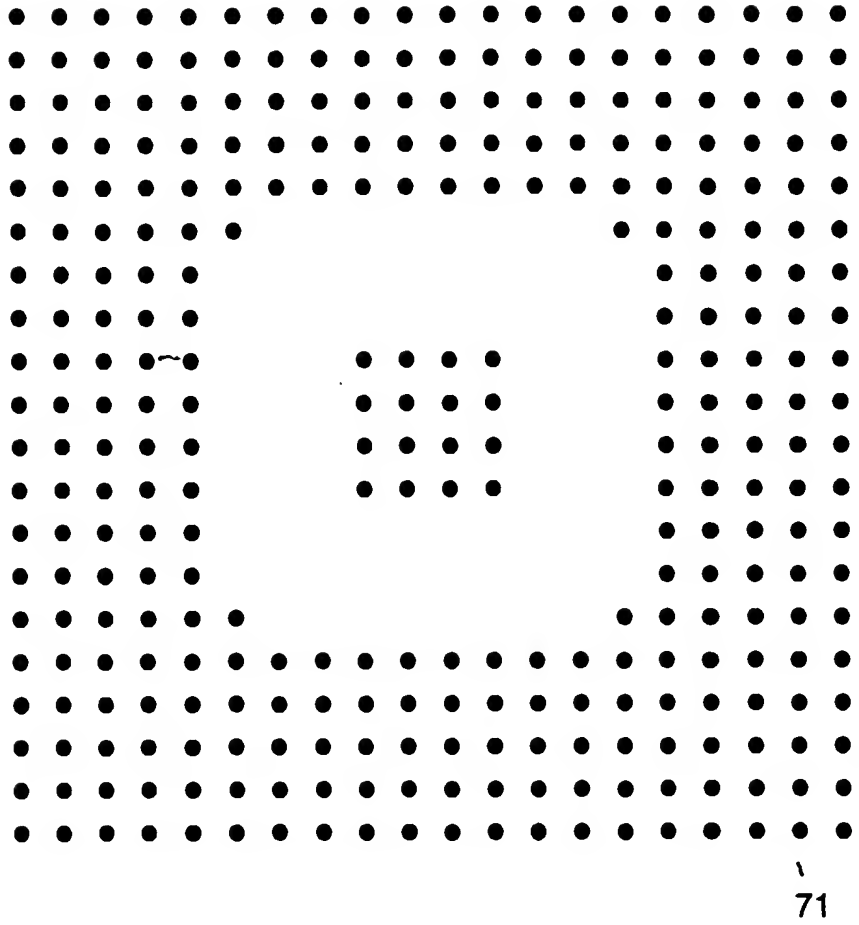


FIGURE 4

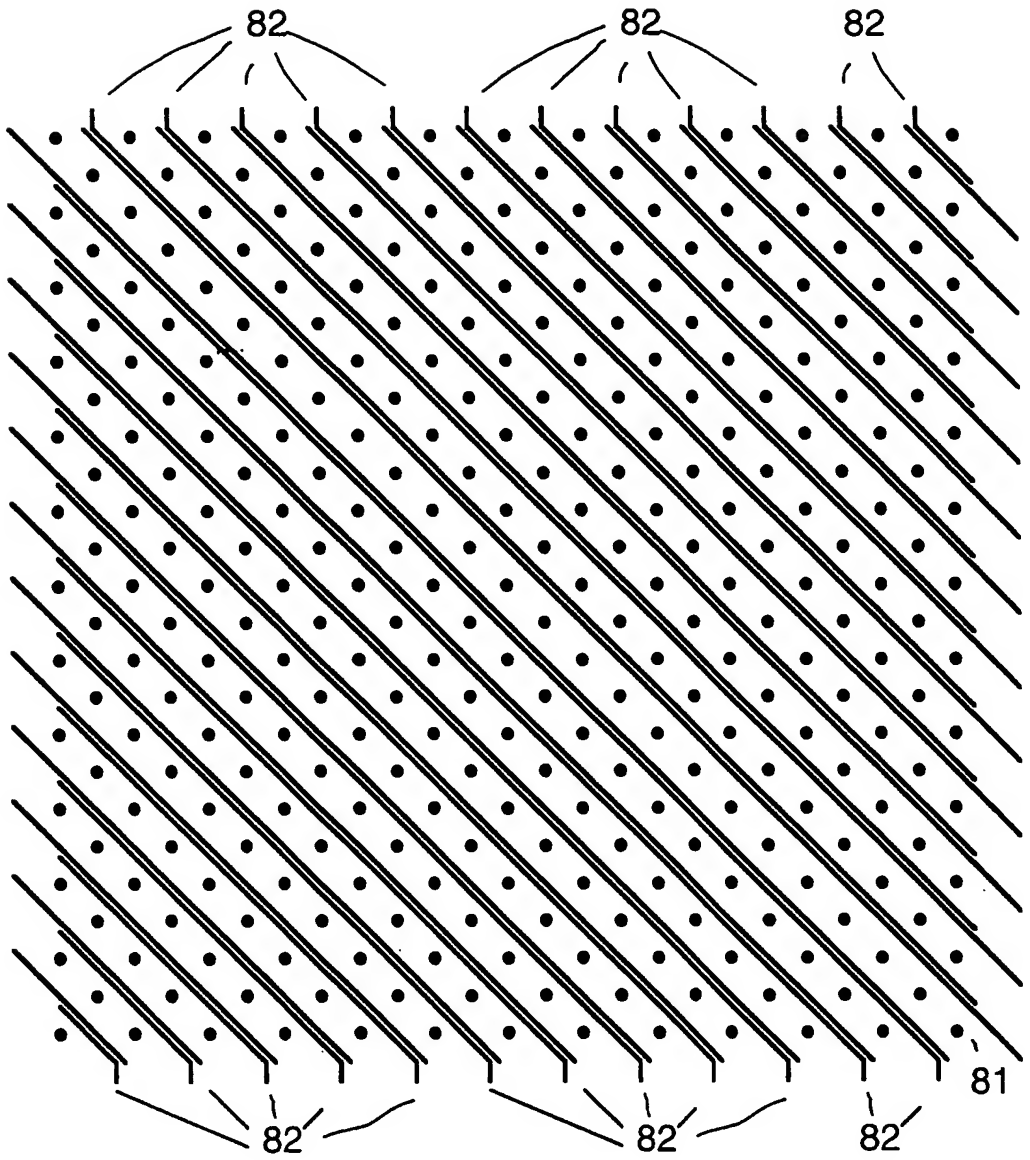


FIGURE 5

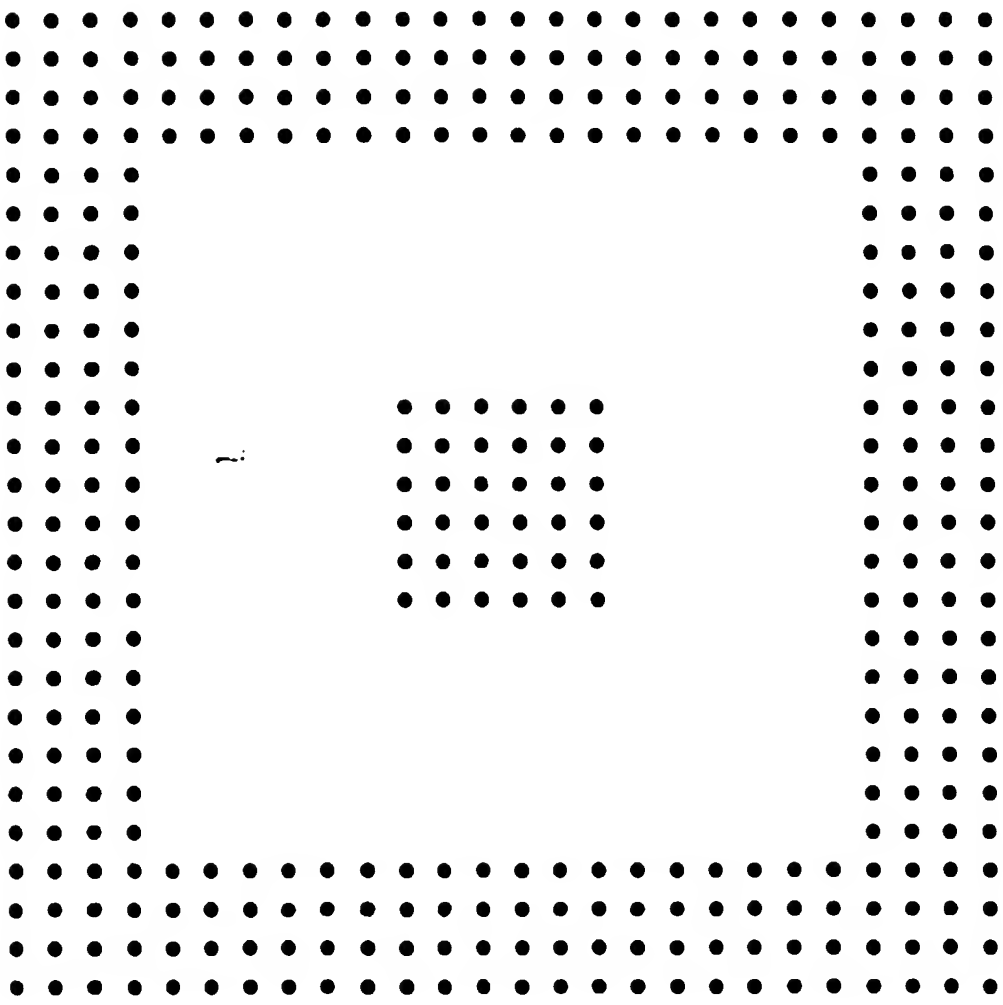


FIGURE 6

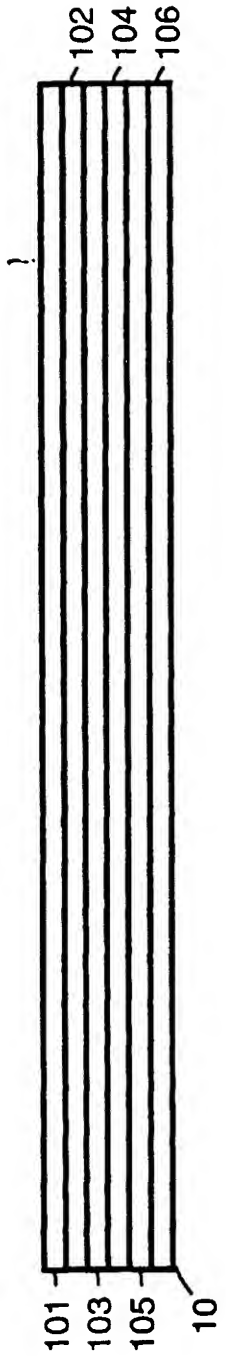


FIGURE 7